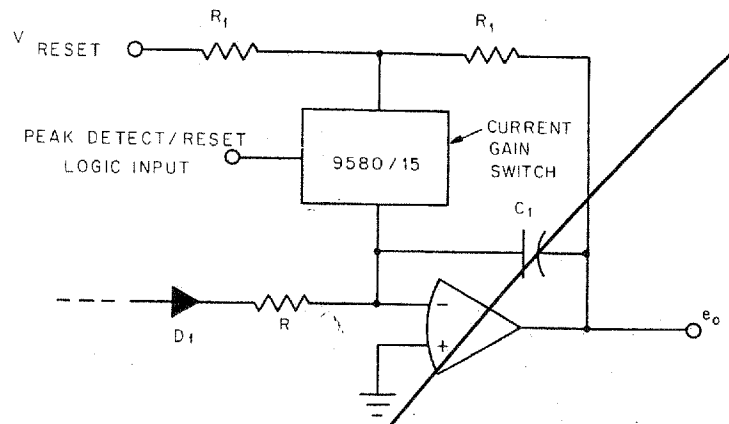

Fig. 9.28 Fast reset circuit for inverting-type peak detectors.

switches. If fast resetting is needed, C_1 and the ON resistance of SW_2 must be as small as practical. Another method of implementing the HOLD mode is to place a switch in series with the input signal to "gate" it to OFF. When only the PEAK DETECT and RESET modes are needed, switch SW_1 can be eliminated if SW_2 has very low impedance such as that of relay contacts. Figure 9.28 shows a very fast method for resetting the inverting-type peak detectors with a current-gain sample-hold switch. (See Sec. 9.4.)

This circuit has the advantage that the switch in series with D_1 is not necessary since the sample-hold switch has very low output impedance. To reset C_1 to 0 V, V_{RESET} must be zero. Capacitor C_1 can be reset to +10 V by making V_{RESET} equal to −10 V so that input peaks can be detected over the full −10 to +10 V range.

9.5.5 Peak-to-peak detector Figure 9.29a shows a method for measuring the peak-to-peak value of a signal that swings both positive and negative in amplitude. If only positive peak detectors are available, the circuit can be built using one extra amplifier as shown in Fig. 9.29b.

9.6 Comparators[15–17]

Comparators are used as analog/digital (hybrid) building blocks, since the digital output signal is simply the answer to the question: Is the analog input signal greater than or less than the analog reference signal? The input and reference signals can come from voltage or current sources or from a combination of the two types of sources. When operational amplifiers are used as comparators, there are usually one or more summing resistors connected to the inverting input (summing junction) of the operational amplifier. One can think of the circuit as comparing currents

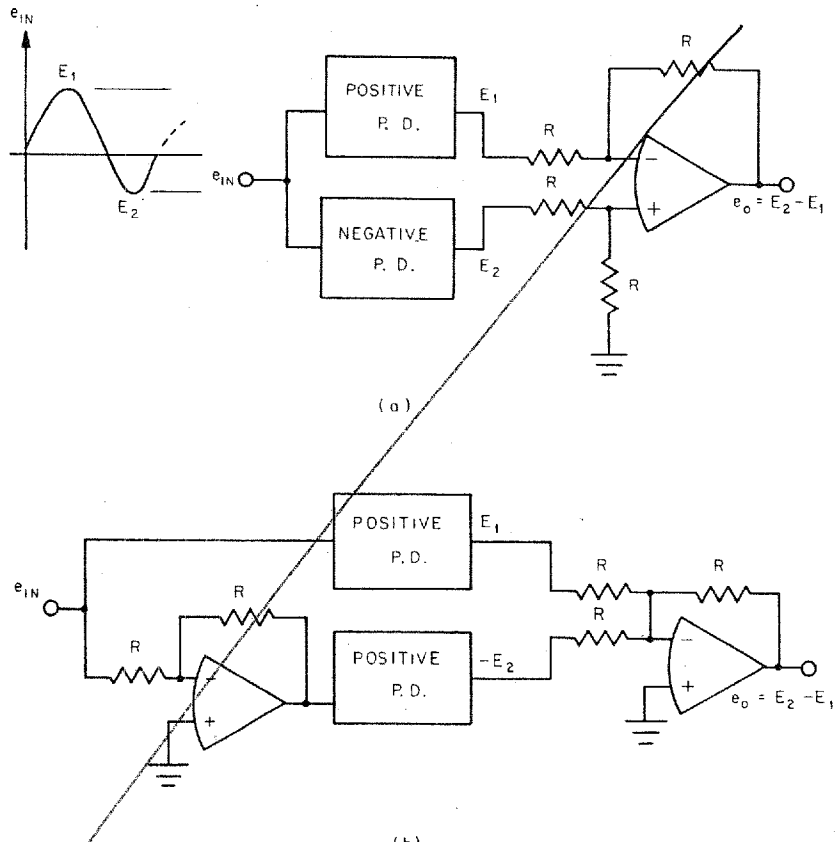

Fig. 9.29 Peak-to-peak detector circuits: (a) using one positive and one negative peak detector; (b) using two positive peak detectors.

or voltages. In this section we shall consider several types of such comparators.

9.6.1 Zero-crossing detector The simplest comparator is the zero-crossing detector which answers the question: Is the input signal greater than or less than zero? A typical circuit for such a detector is shown in Fig. 9.30. The limit circuit shown in the figure produces one output level when i_3 is positive and a different output level when i_3 is negative. Since the limit circuit changes state when i_3 changes sign, the comparison point occurs when $i_3 = 0$ as shown below (assume the summing junction potential is zero):

$$i_1 = I_2 + i_3 \tag{9-2}$$

$$\frac{e_1}{R} = I_2 + i_3 \tag{9-3}$$

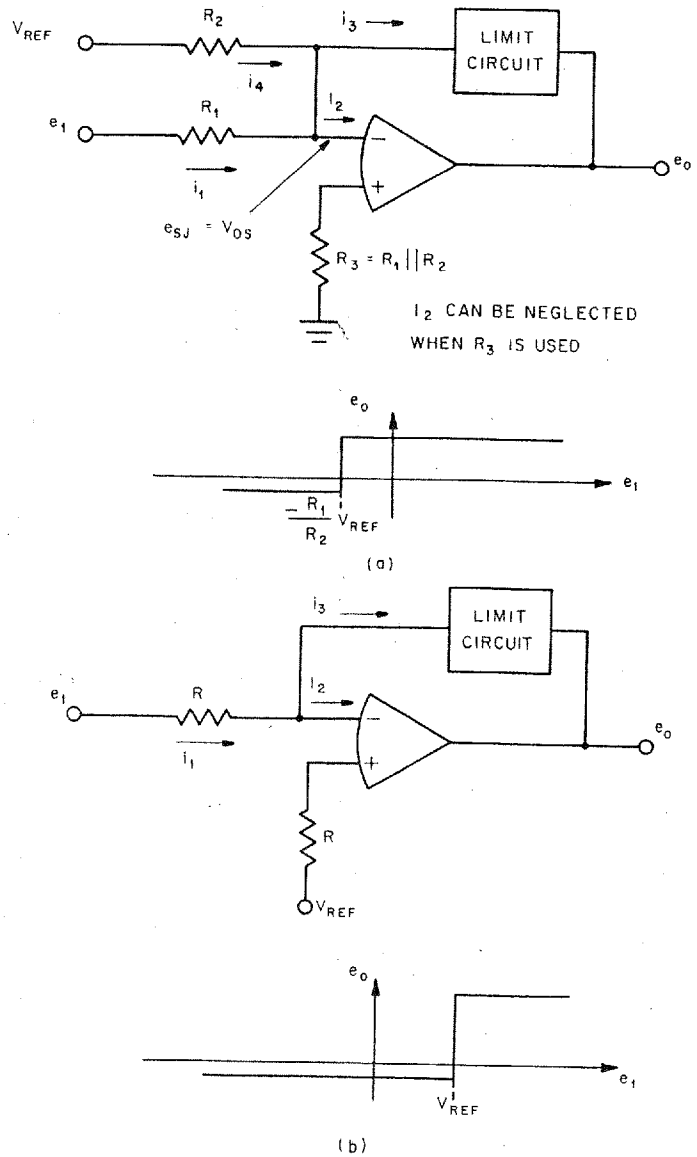

Fig. 9.31 Two-level detector circuits: (a) summing type; (b) differential type.

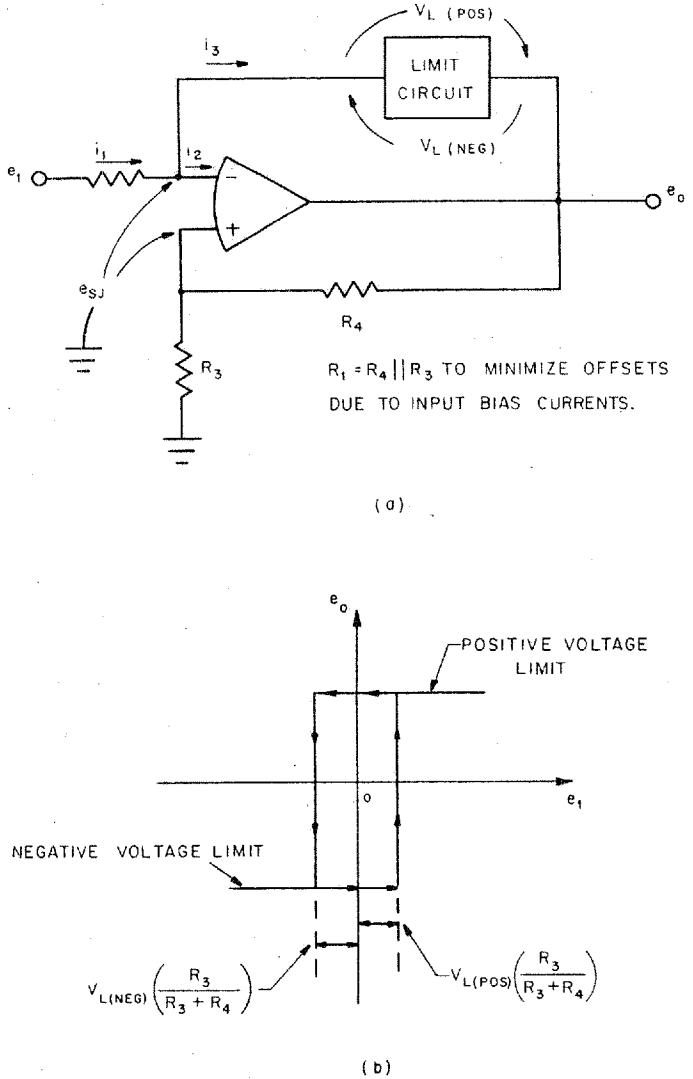

Fig. 9.32 Zero-crossing detector with hysteresis. (a) Circuit diagram; (b) transfer curve.

but

$$e_o = e_{SJ} \pm V_L$$

Thus

$$e_{SJ} = \pm V_L \frac{R_3}{R_4} \qquad \text{(hysteresis)}$$

and

$$e_o = \pm V_L\left(1 + \frac{R_3}{R_4}\right)$$

If hysteresis is added to the circuits of Fig. 9.31a and b, the hysteresis can still be calculated by using the above equations, except that the hysteresis will be centered about $-(R_1/R_2)V_{REF}$ in Fig. 9.31a and about V_{REF} in Fig. 9.31b. The disadvantage of using hysteresis is that the comparison points do not occur at the zero reference or level. Therefore, a tradeoff must be made between the degree of noise immunity required and the error at the comparison points. Prefiltering the input signal to reduce the input noise may be helpful. In order to have symmetrical comparison points about zero, the output voltage limits must be equal in magnitude. In some applications the positive and negative limits will not be the same magnitude, resulting in asymmetry about the nominal comparison point.

9.6.3 Window comparator The final type of comparator that we shall consider in this section is the window comparator. Figure 9.33 shows the circuit diagram and the transfer function for such a comparator. The center of the window is set by the negative of the input V_2, and the window width is twice the input ΔV. Thus the window can be shifted while maintaining constant window width by varying only one voltage (V_2). This feature is useful for probability studies (see Fig. 9.34) where the window width is swept at a constant rate across the analog input range. Similarly, the window width can be varied by a single voltage, without affecting the center of the window.

The window comparator operates in the following way. When $e_1 + V_2 < 0$, D_2 of A_1 is conducting and D_1 is reverse-biased. Therefore the output of A_1 does not contribute to the output of A_2 since the voltage at the junction of R/2 and R/4 is zero. The limiter circuit of A_2 changes sign when the current i_d changes sign, or

$$\frac{e_1}{R} + \frac{V_2}{R} + \frac{\Delta V}{R} = i_d = 0 \qquad (9\text{-}9)$$

so that

$$e_1 = -V_2 - \Delta V \qquad (9\text{-}10)$$

Equation (9-10) gives the lower comparison point of the window. When $e_1 + V_2 > 0$, D_1 will be conducting so that the output of A_1 will be $-\frac{1}{2}(e_1 + V_2)$. Another comparison point will be given by

$$\frac{e_1}{R} + \frac{V_2}{R} + \frac{\Delta V}{R} - \frac{\frac{1}{2}(e_1 + V_2)}{R/4} = i_d = 0 \qquad (9\text{-}11)$$

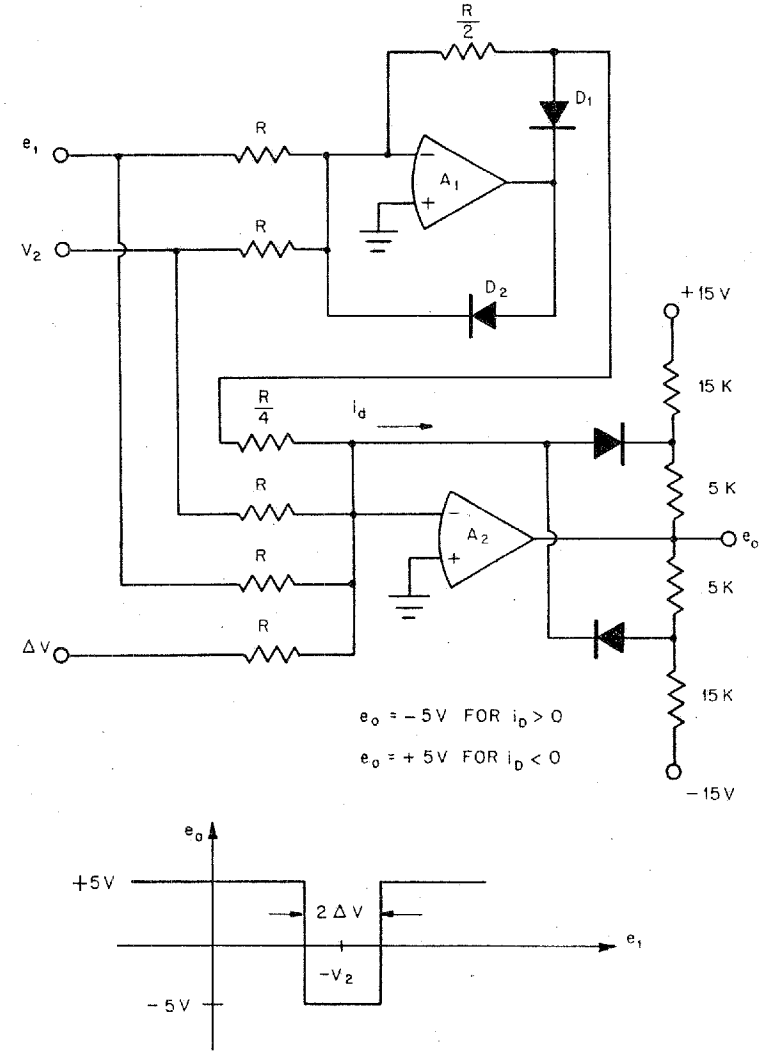

Fig. 9.33 Circuit diagram for a window comparator.

so that

$$e_1 = -V_2 + \Delta V \qquad (9\text{-}12)$$

which is the upper comparison point.

By adding the appropriate logic gates at the outputs of A_1 and A_2 a window comparator can be given three logic outputs called the GO, HIGH, and LOW outputs. Whenever the input signal is inside the

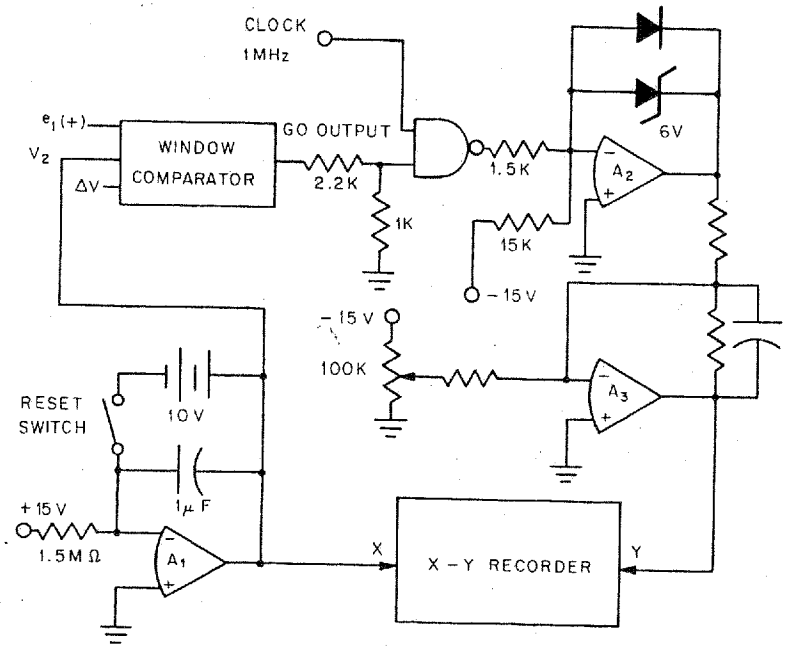

Fig. 9.34 Probability density analyzer.

window, the GO output will be a logical 1 and the other two outputs will be at a logical 0. If the input signal drops to a value below the window, the LOW output will switch to a logical 1 and the GO output will drop to a logical 0. When the input signal exceeds the window, the HIGH output will be at a logical 1 and the other outputs at a logical 0.

The window comparator is shown in Fig. 9.34 as part of a probability density analyzer. The GO output of the window comparator goes to HIGH each time the input signal is inside the window. When the clock and the GO output are both HIGH, the output of the first NAND goes to LOW. A_2 is a comparator that is used to generate precision voltage levels for the RC averaging filter. The 100 kΩ potentiometer is adjusted to null the offset, since the LOW output of A_2 is not 0 V. A_1 is connected as an integrator that sweeps the window center from −10 to +10 V at a rate of 1 V/s. The window width (2 ΔV) and the rate the window is swept will be a function of the input being analyzed.[1]

9.6.4 Amplitude classifier Often it is required to sort items into many different bins. An example of this is grading apples into different groups according to size. Figure 9.35 shows how a system can be implemented

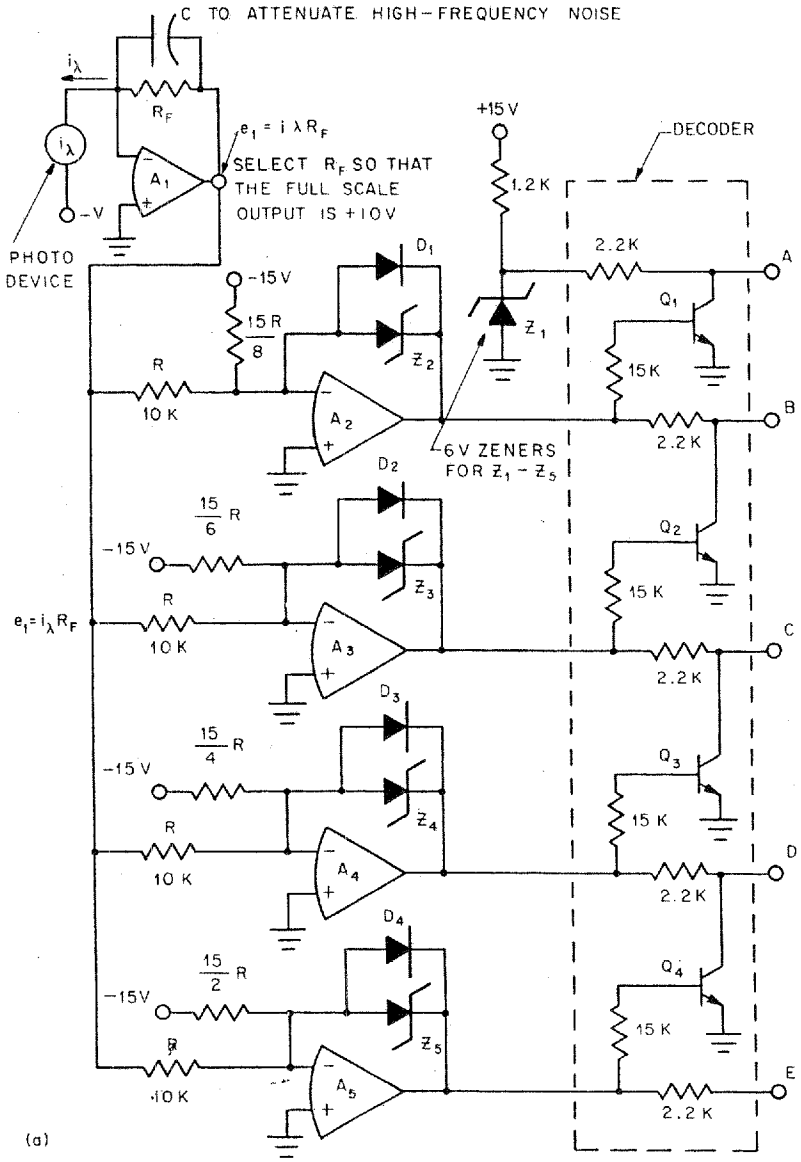

Fig. 9.35 Five-level amplitude classifier. (a) Circuit diagram.

INPUTS e_1	OP AMP OUTPUTS Z_1	A_2	A_3	A_4	A_5
$8 < e_1 \leq 10$	1	0	0	0	0
$6 < e_1 \leq 8$	1	1	0	0	0
$4 < e_1 \leq 6$	1	1	1	0	0
$2 < e_1 \leq 4$	1	1	1	1	0
$0 \leq e_1 \leq 2$	1	1	1	1	1

FOR OPERATIONAL AMPLIFIER OUTPUTS

LOGICAL 1 = 6 V
LOGICAL 0 = .6V

DECODER OUTPUTS A	B	C	D	E
1	0	0	0	0
0	1	0	0	0
0	0	1	0	0
0	0	0	1	0
0	0	0	0	1

DECODER OUTPUTS

LOGICAL 1 = 6 V
LOGICAL 0 = 0 V

(b)

Fig. 9.35 (b) Table of output codes.

by using operational amplifiers as comparators. Amplifier A_1 operates as a current-to-voltage converter for the light-sensitive photodiode array which is used to detect the size of the apples. Amplifiers A_2 to A_5 operate as biased comparators with a simple clamp circuit. The decoder ensures that only one logic output is at HIGH at a time. This decoder can drive TTL (transistor-transistor logic) or DTL (diode-transistor logic) directly or an n-p-n switching transistor which can control larger currents such as the coil current of a relay. Hysteresis can be added to each of the comparators for noise immunity if desired.

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